Printed Pages:02 **Sub Code: KEE401**

Paper Id: 238345 **Roll No.** | | | | | | | | | | |

B.TECH.
(SEM IV) THEORY EXAMINATION 2022-23
DIGITAL ELECTRONICS

Time:3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data then choose suitably.

SECTION A

1. Attempt *all* questionsinbrief. 2 x 10 = 20

(a) Explain Duality Principle. Prove that positive logic AND Gate is equivalent to negative logic OR Gate.
(b) Explain 2-input EX-NOR Gate and implement it using minimum number of 2-input NOR Gates.
(c) Explain Half adder circuit and implement it using 2-input NAND Gates.
(d) Write down the differences between Combinational and Sequential digital circuits.
(e) Differentiate between Synchronous and Asynchronous sequential circuits.
(f) Explain in brief:- (i) Astable Multivibrator (ii) Bistable Multivibrator.
(g) Explain the working of a PISO type shift register briefly.
(h) What are Static and Dynamic Hazards?
(i) What is Noise Margin?
(j) What are the advantages of CMOS logic family?

SECTION B

2. Attempt any *three* ofthefollowing: 10x3=30

(a) Find the Simplified logical expression for Y.
$Y(A,B,C,D,E) = \sum m(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)$.
(b) Implement a 1:8 De-mux with selection lines A,B,C using 1:2 De-mux. Verify your implementation with the help of Truth Tables.
(c) What is Race-Around condition in J-K flip-flop? Explain it's solution Master- Slave J-K Flip-Flop.
(d) Given the conditions, such that If input A = 0, the circuit oscillates between either one of the two cases. Case1:- 00-01-00-01 and Case2:- 10-11-10-11 And If A = 1, it switches inter between two cases. Draw the state transition diagram and implement the same using JK flip-flop and by using basic logic gates.
(e) Implement a 3-input NOR Gate using CMOS and DTL logic families. Also Explain the working in both cases.

SECTION C

3. Attempt any *one* part ofthe following: 10x1=10

(a) Implement NOT, OR, AND , EX-OR, EX-NOR, NOR (all 2-inputs except NOT Gate) gates using minimum number of 2-input NAND Gates.
(b) Convert all possible 4-bit binary codes into Gray Code. Also show the implementation circuit using 2-input EX-OR Gates only.

4. Attempt any *one* part ofthe following: 10x1=10

(a) Implement a circuit using logic gates that compares the magnitudes of two 4- bit numbers.

(b) Implement the Boolean function F(A,B,C,D)=∑m(0,1,2,5,8,13,14) using 8:1 MUX with A,C,D as selection lines.

5. Attempt any *one* part ofthe following: 10x1=10

(a) Implement S-R, T, D flip-flops using J-K flip-flop. Also show the implementation with help of State Tables.

(b) Design a MOD-12 asynchronous down counter using T flip-flops.

6. Attempt any *one* part ofthe following: 10x1=10

(a) Given a sequential logic circuit expression as X(t+1) = p'X + pY Y(t+1) = pX'+p'Y where X and Y are the two flip-flop outputs and pis the main external input. Draw the state transition table for the above- given logic function. Also, draw the state transition diagramassociated
with it.

(b) Design a synchronous3-bitFSM (which can be used for counting) using D flip-flops with no external inputs and count sequence as follows:- 0- 1-3-7-4-2-0.

7. Attempt any *one* part ofthe following: 10x1=10

(a) Explain Propogation delay in logic families. Also explain why $T_{PLH} > T_{PHL}$.

(b) Explain ROM and its various types. Implement a 4-T SRAM cell using MOSFETs.